REMARKS

Claims 1 – 34 are pending. Claims 1 – 25 and 33 are allowed, and the Applicants' attorney has amended claims 26 and 27. As discussed below, claims 26-32 and 34 are now in condition for allowance.

The Assignee will surrender the original patent, or submit a declaration as to the loss or inaccessibility of the original patent, after the Examiner allows all of the claims.

Rejection of Claims 26, 28-32, and 34 Under 35 U.S.C. § 103 in View of FIG. 1 of the Reissue Application (Reissue of U.S. Patent 5,710,461)

The Applicants' attorney has amended claim 26 to recite in part "an interlevel dielectric disposed on the second conductive layer and including three insulating layers, two of the three insulating layers being separately planarized spin-on glass layers." This limitation is similar to respective limitations in the allowed claims 7 and 12, and thus renders claim 26 allowable without raising new issues that would require further consideration and an additional search by the Examiner. Therefore, the Applicants' attorney requests the Examiner to enter this amendment and to allow the reissue application.

Claim 27 Contains Allowable Subject Matter

Therefore, the Applicants' attorney has amended claim 27 as an independent claim.

CONCLUSION

In addition to the allowed claims 1 – 25 and 33, claims 26 – 32 and 34 are in condition for allowance, and that action is requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully submitted,

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ALL PENDING CLAIMS INCLUDING MARKED UP VERSION OF AMENDED CLAIMS

Marked up version of amended claims 26, 27:

1. An integrated circuit SRAM cell, comprising:

a substrate which includes at least one substantially monolithic body of semiconductor material;

a first patterned thin-film layer comprising polysilicon;

a second patterned thin-film layer comprising polysilicon and overlying said first thin-film layer, said second layer being doped to provide high conductivity;

a patterned interlevel dielectric overlying portions of said first and second thin-film layers, said interlevel dielectric including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers including a lower portion of a spin-on glass a middle portion of a dielectric material which is not spin-on glass, and an upper portion of spin-on glass;

a third patterned thin-film layer comprising polysilicon having a very high resistivity;

wherein said first patterned thin-film layer is configured to provide transistor gates, and said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide resistive loads for each said latch.

Claims 2-6: see issued patent.

7. An integrated circuit SRAM cell, comprising:

first and second overlaid thin-film conductor layers, each comprising clad polysilicon, at least one of said conductor layers being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying portions of said second thin-film layer, and including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

a third patterned thin-film layer comprising polysilicon having a very high resistivity, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide passive loads for respective ones of said latches.

Claims 8-11: see issued patent.

12. An integrated circuit SRAM cell, comprising:

at least one patterned thin-film conductor layer comprising polysilicon and being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying said at least one patterned thin-film conductor layer, and including multiple independently planarized layers of dielectric materials therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

an additional patterned thin-film layer comprising polysilicon, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said at least one patterned thin-film conductor layer is interconnected to provide an array of latches, and said additional thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said conductor layers to provide passive loads for respective ones of said latches.

Claims 13-18: see issued patent.

19. The integrated circuit SRAM cell of claim 1 wherein the third patterned thin-film layer comprises substantially undoped polysilicon.

20. The integrated circuit SRAM cell of claim 19 wherein the substantially undoped polysilicon comprises intrinsic polysilicon.

21. The integrated circuit SRAM cell of claim 1 wherein the third patterned thin-film layer comprises a polysilicon layer doped with chlorine.

22. The integrated circuit SRAM cell of claim 7 wherein the third patterned thin-film layer comprises substantially undoped polysilicon.

23. The integrated circuit SRAM cell of claim 22 wherein the third patterned thin-film layer comprises intrinsic polysilicon.

24. The integrated circuit SRAM cell of claim 7 wherein the third patterned thin-film layer comprises a polysilicon layer doped with chlorine.

25. The integrated circuit SRAM cell of claim 12 wherein the third patterned thin-film layer comprises substantially intrinsic polysilicon.

26. (Three Times Amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

~~a plurality of separately planarized spin-on glass layers~~ an interlevel dielectric disposed on the second conductive layer and including three insulating layers, two of the three insulating layers being separately planarized spin-on glass layers;

an insulating layer disposed on [a top one of the planarizing spin-on glass layers] the interlevel dielectric; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

27. (Three Times Amended) [The] An integrated circuit SRAM cell [of claim 26] formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of separately planarized spin-on glass layers disposed on the second conductive layer;

an insulating layer disposed on a top one of the planarizing spin-on glass layers;

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches; and

wherein the plurality of separately planarized spin-on glass layers includes a first spin-on glass layer disposed on the second conductive layer, an oxide layer disposed on the first spin-on glass layer, and a second spin-on glass layer disposed on the oxide layer.

28. The integrated circuit SRAM cell of claim 26 wherein each of the conductive layers comprises a suitably doped polysilicon layer.

29. The integrated circuit SRAM cell of claim 26 wherein the first conductive layer comprises a first polysilicon layer and a cladding layer formed on the first polysilicon layer.

30. The integrated circuit SRAM cell of claim 29 wherein the cladding layer comprises tantalum silicide.

31. The integrated circuit SRAM cell of claim 26 wherein the second conductive layer comprises a second polysilicon layer and a cladding layer formed on the second polysilicon layer.

32. The integrated circuit SRAM cell of claim 31 wherein the cladding layer comprises tantalum silicide.

33. An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of planarizing spin-on glass layers disposed on the second conductive layer;

an undoped oxide layer disposed on a top one of the planarizing spin-on glass layers; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

34. The integrated circuit SRAM cell of claim 26 wherein the third conductive layer comprises intrinsic polysilicon.